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graph TD
    2[Generate Clocks] --> 4[Transmit Clocks To Receiving Device]
    4 --> 5[Generate Sync Signal]
    5 --> 6[Designate Sync Test Line]
    6 --> 8[Transmit Data Over Data Lines]
    8 --> 10[Receive & Sample Sync Signal At Receiving Device To Produce Sample Data Sets]
    10 --> 12[Compare Sample Data Sets To 1st Phase Sync Detect Patterns]
    12 --> 14[Store 1st Time Delay Values]
    14 --> 16[Compare Sample Data Sets To 2nd Phase Sync Detect Pattern]
    16 --> 18[Store 2nd Phase Time Delay Value]
    18 --> 20[Sample Future Data Streams On Designated Data Lines At 1st & 2nd Phase Time Delay Values]
    20 --> 22[Designate New Sync Test Line]
    22 --> 24[Calculate Associated 1st & 2nd Phase Time Delay Values For Each Data Line]
    24 --> 26[Sample Data Streams at Associated 1st & 2nd Phase Time Delay Values]

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Fig. 1

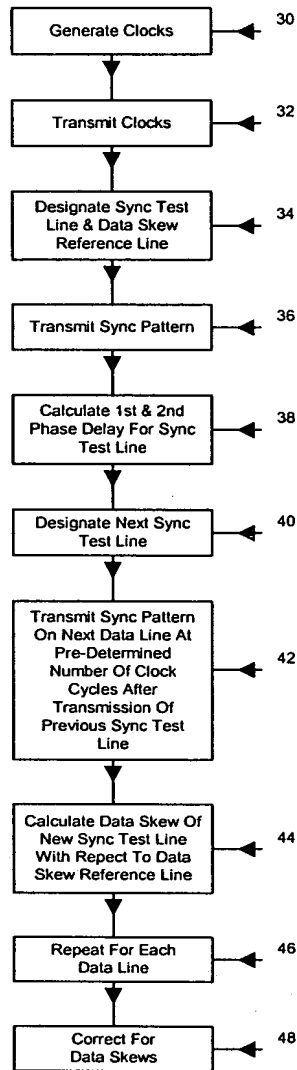


Fig. 2

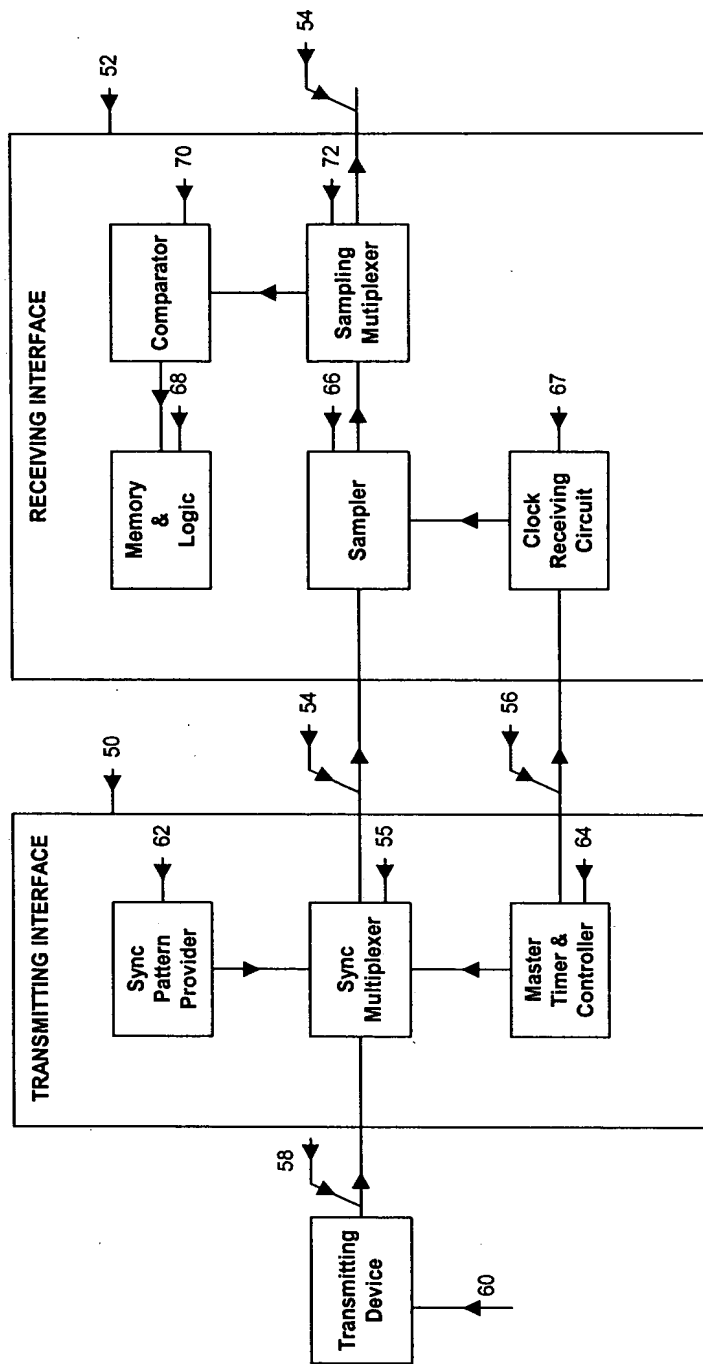


Fig. 3

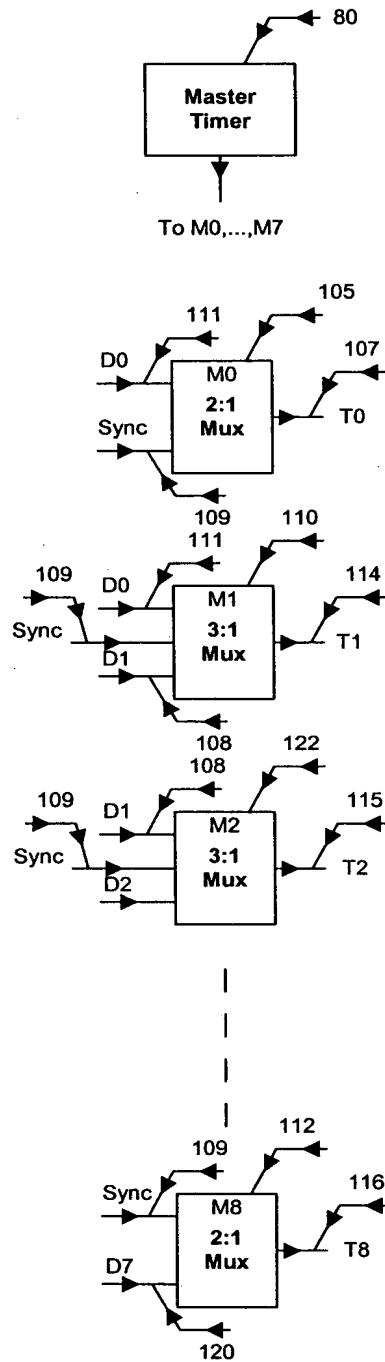


Fig. 4

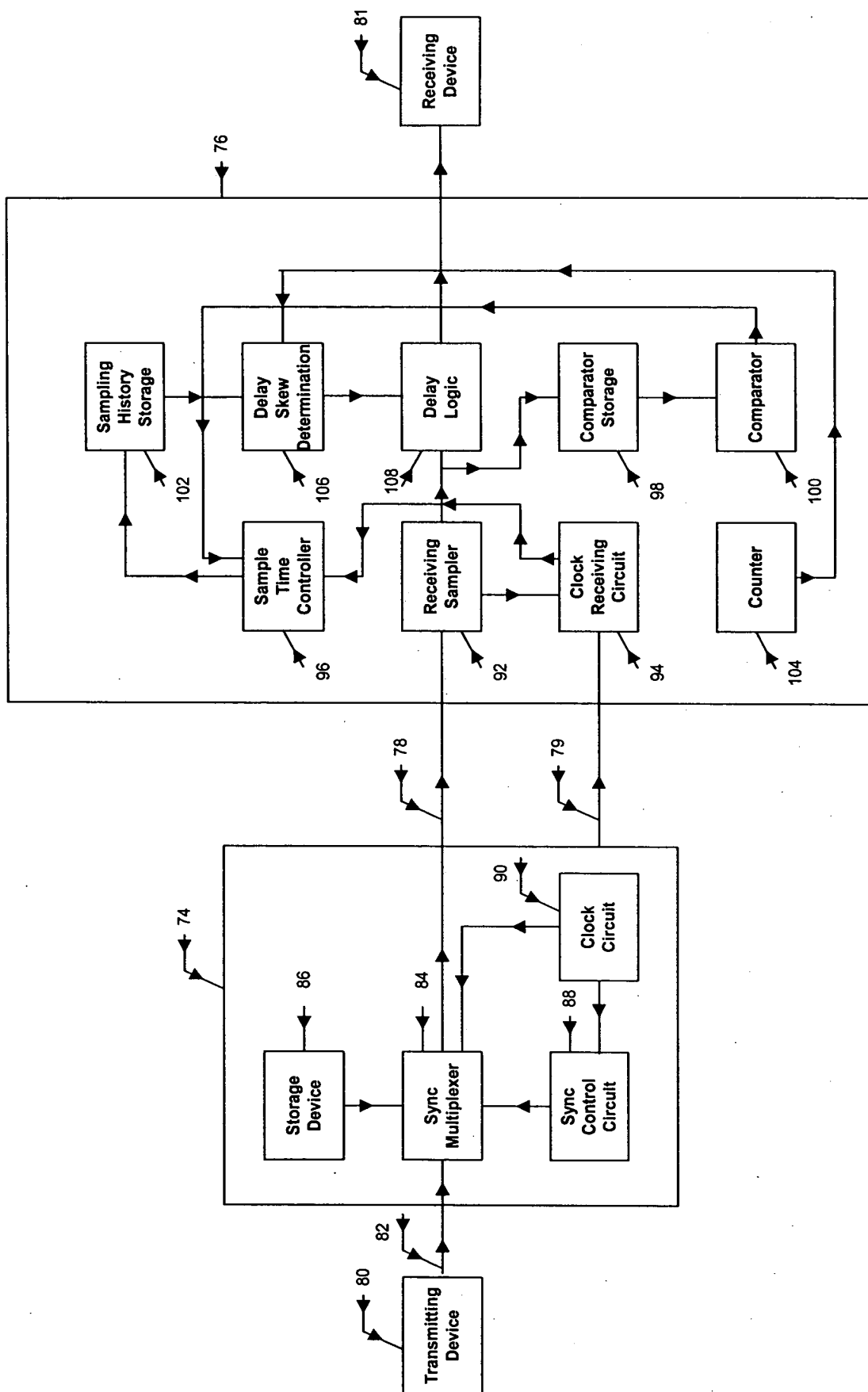


Fig. 5

The diagram illustrates a multi-channel system with two identical processing units, M0 and M8, connected by a dashed line. Each unit consists of a 10:1 Mux, a Storage Register, and a final Mux. The 10:1 Mux in each unit receives inputs from a common bus (128) and a local input (130). The output of the 10:1 Mux (134) is fed into a Storage Register (138), which is clocked by a common Clock signal (132). The output of the Storage Register (140) is fed into a final Mux, which also receives a local input (140). The final output of the system is 126.

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